31.1 A Single-Chip Bluetooth EDR Device in 0.13µm CMOS

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Since the release of the initial Bluetooth specifications, the demand for higher data transmission capacity has recently led to the standardization of the enhanced-data-rate (EDR) mode. In addition to the basic 1Mb/s rate using GFSK modulation, π/4-DQPSK modulation for 2Mb/s and 8-DPSK modulation for 3Mb/s mode have been included. Fully integrated basic rate non-EDR [1][2] and EDR compliant [3] Bluetooth transceivers have previously been reported. In this paper, the architecture of a Bluetooth EDR-compliant transceiver, implemented in a 0.13µm CMOS technology, is presented. This SoC operates in the unlicensed 2.4GHz ISM band and integrates the complete radio together with the digital baseband.

The transceiver architecture is shown in Fig. 31.1.1 and employs a low-IF image-reject receiver, a direct-up conversion transmitter, and a fractional-*N* synthesizer followed by a $3\times f_{VCO}/2$ local-oscillator-generation scheme [4]. The RF signal passes through a configurable transformer circuit which is shared between the receiver and transmitter. On the receiver side a variable-gain LNA amplifies the RX signal before the downconversion mixer stage. After the mixer, a variable-gain polyphase band-pass filter performs partial channel selection and image rejection. The IF signal is then digitized by a continuous-time ΔΣ band-pass ADC (CT-ΔΣ ADC) before further signal processing is performed in the digital domain which includes functions such as additional channel-select filtering, RSSI estimation, automatic gain control (AGC), and demodulation.

The symbols to be transmitted are first processed by a pulse-shaping filter followed by I/Q baseband modulation and ΔΣ noise shaping. The digital quadrature signals are converted into the analog domain by the I/Q DACs followed by low-pass filtering and upconversion by the I/Q mixer. After the mixer stage the modulated RF signal is amplified by a variable-gain power amplifier (PA) and then passed through the shared transformer circuit out to the antenna.

The SoC integrates additional analog blocks such as low drop-out (LDO) supply regulators, R- and RC-calibration circuitry, a temperature sensor, a low-power oscillator (LPO), a crystal oscillator (XO), and an integrated IF-PLL which generates clocks for the receiver ADC, transmitter DACs, and digital blocks. To complete the system additional digital blocks such as CPU, memory, UART, and USB interfaces are included as parts of the digital baseband which handles all the necessary Bluetooth link functions.

The RF front-end transformer, LNA, and PA are depicted in Fig. 31.1.2. The TX/RX transformer circuit [5] couples the signal from its primary to its secondary side which connects directly to the inputs of the LNA and outputs of the PA. Depending on the mode of the NMOS switches controlled by EN_P and EN_N, either RFN or RFP can be tied to ground and the opposite port will be selected as the RF input/output. Each switch contributes to about 1dB signal loss in RX or TX mode and enhanced performance can be achieved by additional external port grounding. Because of the fully balanced front-end design the transformer circuit can also be configured as a differential port. The transformer and its load are forming a parallel resonance circuit and are designed to have a real impedance of about 50Ω at the primary terminals around the operating frequency. When the LNA or PA are off they provide a high-impedance load at the secondary side of the transformer and the TX/RX switch functionality is inherent in the topology by having either the PA or LNA enabled at any given time. The LNA is a fully differential cascode amplifier with an LC load at the output. As the impedance matching is defined by the transformer circuit, the input capacitance of the LNA is considered as a part of the total capacitance needed for the transformer to resonate at the desired frequency. The LNA incorporates gain control in 3dB steps implemented by a current steering mechanism in the cascode devices.

The PA gain stage is a pseudo-differential cascode amplifier. Variable output power in 2dB steps is implemented by splitting the transistors in weighted branches with each branch enabled by a cascode device. The output currents from all branches are then summed at the transformer secondary port. In TX mode, the terminals of the LNA NMOS input device are weakly biased to ground and the voltage swing is always below the maximum rated voltage to ensure long-time reliability.

The direct-upconversion transmitter circuit is depicted in Fig. 31.1.3. The digital I and Q signals are noise shaped in the digital domain to relax the SNR requirements of the transmit DACs. The ΔΣ noise shaping together with an oversampled 4b current-steering DAC provides an overall 11b resolution in the desired 1MHz signal band. Each single-ended DAC output current is first converted to voltage through a diode-connected NMOS transistor followed by a low-pass filter and a mixer transconductance input stage. The filter rejects any unwanted out-of-band noise and is implemented as a passive 3-stage low-pass topology with a 3dB cut-off at around 2MHz. To improve the overall transmitter linearity the harmonics generated by the nonlinear current-to-voltage transfer characteristic of the diode-connected NMOS device should be kept as low as possible, as the higher-order harmonics will be filtered out before the signal current is reconstructed at the mixer input stage. Therefore, resistive degeneration is included in the mirroring NMOS devices.

The frequency-upconversion stage is using a double-balanced mixer topology. Identical DAC, filters, and upconversion circuits are used for both I and Q paths. The output currents of the upconversion mixers are summed which results in the necessary single-sideband mixing. At the output of the mixers a tuned LC-resonator provides the load. All together, the digital noise shaping together with low-order DACs and passive low-pass filter topology results in an area efficient transmitter implementation with low power consumption.

On the RX side analog-to-digital conversion is performed by the CT-ΔΣ ADC circuit which is depicted in Fig. 31.1.4. The 2^{nd}-order CT band-pass ΔΣ consists of two integrators, a 4b quantizer, and two 4b feedback DACs. The topology is optimized for a clock frequency of 48MHz and achieves 66dB peak SQNR in a 1MHz signal band centered at the IF.

In Fig. 31.1.5 the measured transmitter EVM performance is shown together with the symbol constellation. Measured performance is summarized in Fig. 31.1.6. The radio and analog power consumption in continuous RX mode is about 38mW from a 1.5V supply. The continuous TX power consumption while transmitting at around 3dBm is about 48mW from a 1.5V supply. A die micrograph is shown in Fig. 31.1.7 and the whole transceiver occupies a die area of 11.8mm^2.

References;
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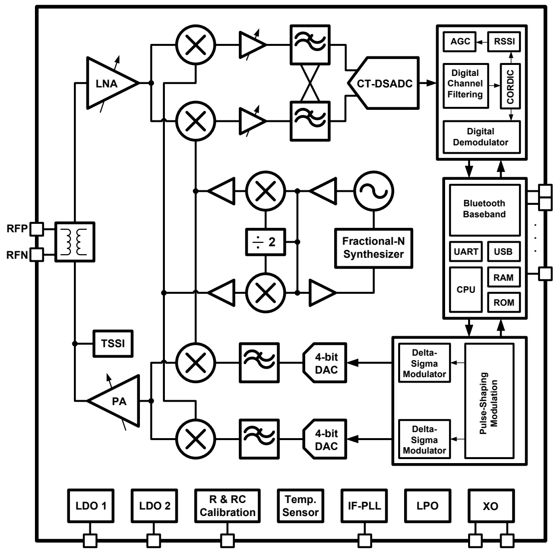

Figure 31.1.1: Single chip Bluetooth EDR transceiver architecture.

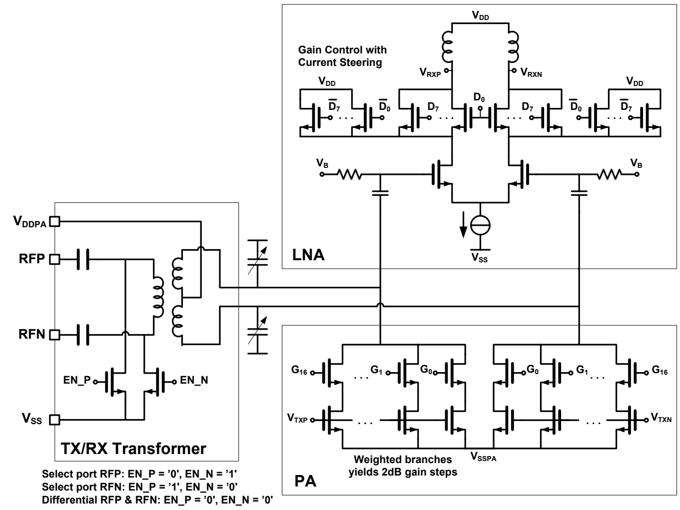

Figure 31.1.2: The Front-End circuit of the Transformer, LNA, and PA.

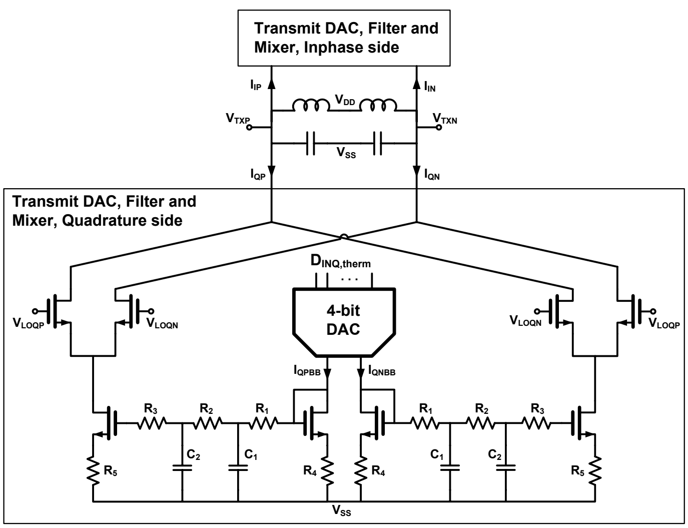

Figure 31.1.3: The transmitter DAC,low-pass filter, and up-conversion mixer.

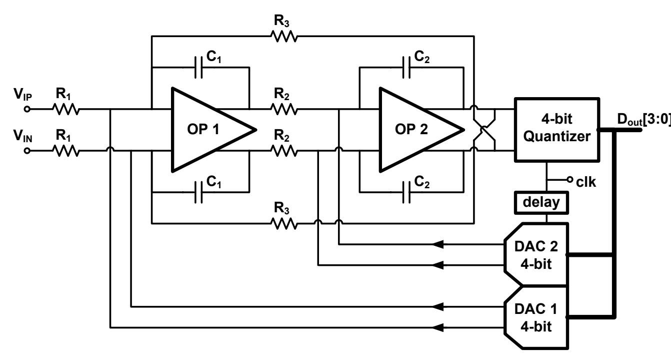

Figure 31.1.4: The continuous- time ΔΣ band-pass ADC circuit used in the receiver.

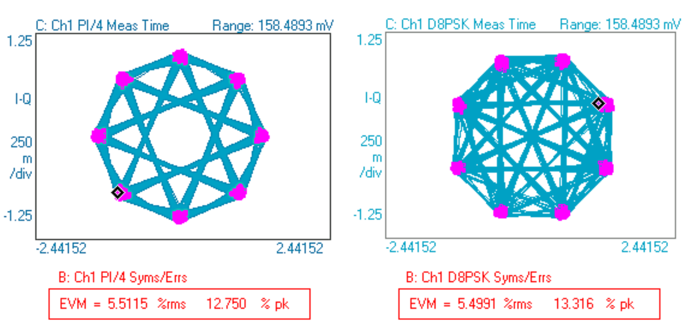

Figure 31.1.5: Measured transmitter EVM performance at 3dBm output power for π/4-DQPSK and 8-DPSK.

Parameter	Measured Data
Supply voltage	1.4V - 1.65V, RF & Digital core 1.7V - 3.6V, Regulator Input and Digital IO
RF/analog supply current Continuous TX Continuous RX	 32mA 26mA
RX sensitivity (2402 to 2480MHz) GFSK (1Mb/s) Pi/4-DQPSK (2Mb/s) 8-DPSK (3Mb/s)	 -88dBm (0.1% BER) < -90dBm (0.01% BER) -84dBm (0.01% BER)
RX chain IIP3, max gain	-18dBm
TX Output Power Nominal Power control	 +3dBm -30dB in 2dB steps
TX DEVM at +3dBm output Pi/4-DQPSK 8-DPSK	 5.5% rms, 12.7% peak 5.5% rms, 13.3% peak
Die Size	11.8mm^2

Figure 31.1.6: Performance summary of the chip.

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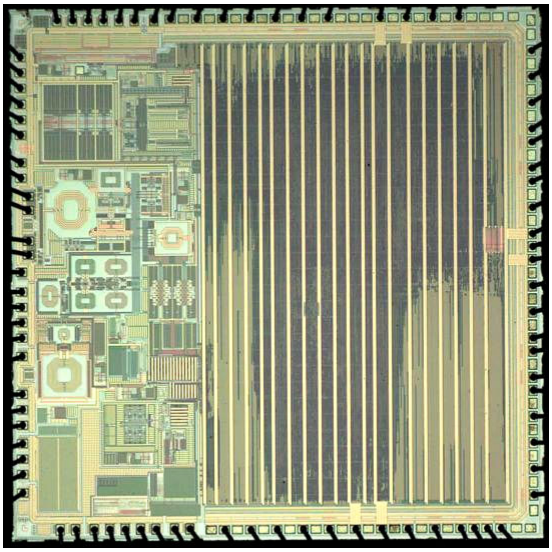

Figure 31.1.7: Chip micrograph.

